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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/075,464	02/15/2002	Shigeru Kawanaka	219713US2	7542
22850	7590	07/28/2005	EXAMINER	
OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314			QUINTO, KEVIN V	
			ART UNIT	PAPER NUMBER
			2826	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/075,464

Applicant(s)

KAWANAKA, SHIGERU

Examiner

Kevin Quinto

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 22 April 2005.
- 2a) ☒ This action is FINAL. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 3-12 and 15-20 is/are pending in the application.
- 4a) Of the above claim(s) 16-20 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 3-7, 9-12, and 15 is/are allowed.
- 6) ☒ Claim(s) 8 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |   |   |
|---|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                        | 4) <input type="checkbox"/> Interview Summary (PTO-413)                     |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)    | Paper No(s)/Mail Date. _____  |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____   | 6) <input type="checkbox"/> Other: _____                                    |

## **DETAILED ACTION**

### ***Response to Arguments***

1. Applicant's arguments with respect to claim 8 have been considered but are moot in view of the new ground(s) of rejection.
2. The examiner notes newly amended claim 8, but has found it to be unpatentable over the prior art of record: Parris et al. (USPN 5,604,700), Venkatasen et al. (USPN 5,736,435), and Yu (USPN 6,534,373 B1). See below for further detail.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Parris et al. (USPN 5,604,700) in view of Venkatasen et al. (USPN 5,736,435) and further in view of Yu (USPN 6,534,373 B1).
5. In reference to claim 8, Parris et al. (USPN 5,604,700, hereinafter referred to as the "Parris" reference) discloses a similar device. Figures 1, 4, and 5 illustrate a semiconductor memory device with a memory cell formed of two transistors on a semiconductor layer. The first and second memory transistors are connected in series with a common wordline. It is understood that one side is connected to a bitline and the

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other side is supplied with a reference potential. Parris does not disclose forming the transistors on an SOI substrate (a semiconductor layer formed on an insulating film). However the use of an SOI substrate is well known in the art. Venkatasen et al. (USPN 5,736,435, hereinafter referred to as the "Venkatasen" reference) discloses that transistors formed on SOI substrates have the advantage of better performance at lower operating voltages than those formed on bulk substrates (column 1, lines 30-38). In view of Venkatasen, it would therefore be obvious to implement the device of Parris onto an SOI substrate. Neither Parris nor Venkatasen discloses implementing partially depleted transistors in the memory cell. However, the use of partially depleted transistors is well known in the art. Yu (USPN 6,534,373 B1) discloses that implementing a partially depleted transistor (such as the device of figure 1) provides the advantages of reduced source-drain junction capacitance and is latch-up free (column 2, lines 1-4). It would therefore be obvious to implement the partially depleted transistors in the memory cell. The examiner notes the new limitation regarding the floating node between the first transistor and the second transistor. However a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In a claim drawn to a process of making, the intended use must result in a manipulative difference as compared to the prior art. See *In re Casey*, 370 F.2d 576, 152 USPQ 235 (CCPA 1967) and *In re Otto*, 312 F.2d 937, 939, 136 USPQ 458, 459 (CCPA 1963). The phrase "wherein a

connection node of said first transistor and said second transistor is in a floating state” does not impose any structural limitation has therefore not been given any patentable weight.

***Allowable Subject Matter***

6. Claims 3-7, 9-12, and 15 were allowed in a previous Office action.
7. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any prior art which suggests using the exact series circuit having partially depleted transistors as described by the applicant.

***Conclusion***

8. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the mailing date of this final action.

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A handwritten signature in black ink, appearing to be "Kevin Quinto", is located in the bottom left corner of the page.